PXIE LEBT Chopper Driver Manual

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1 INTRODUCTION

This following documents the first design for the PXIE LEBT Chopper Driver. It contains the design requirements, some modulator design details and interface control parameters. The design of this first Driver version is for the purpose of commissioning the PXIE LEBT section. It provides the minimum functionality for this purpose.

The LEBT Chopper enables or disables beam to pass to the RFQ. Beam is diverted to the beam absorber with an output voltage of -5 kV applied by the Driver chassis to the deflector plate opposite the absorber plate. An output voltage of 0.0 V allows beam to pass on through.

The Compact Ethernet Communications (CEC) protocol is used for communication between this Driver chassis and an ACNET network node (or any other node such as a LabView application). Section 1 continues to describe the Chopper Driver's specifications and operational features and is intended to be understood by the user for controlling the Chopper Driver. Sections 2 and 3 describes the data needed for communicating with the CEC protocol. Section 4 documents design details.

Changes were made in January 2016 to route user requests for mode setting via the Machine Protection System (MPS) rather than directly. Hardware was added to communicate with the MPS board via TTL serial communications, and C code in the controller was modified to accept mode changes exclusively by the MPS. All other Driver Controller mode functionality remains the same including the way ACNET reads back from the Driver the current operating mode value. Refer to Section 2.2 for more information.

1.1 Specifications

Table 1.1 lists the Chopper Driver's design requirements. All parameters refer to requirements for the driving the Chopper's deflector plate. The absorber plate voltage requirements are not referred to in this document.

Table 1.1. Chopper Driver requirements.

Parameter	Description / Comments	Value	Note
Pulse length	> 90% of maximum intensity	1-16,665 μsec	1
Rise/fall time	10% - 90%	< 0.1 μsec	1
Pulse repetition rate	In either externally triggered or free-running modes DC is provided via a separate operating mode	0 - 60 Hz	1
Output voltage	Voltage to cut beam off	-5.0 kV	1
	Pass-through voltage, option A	0 V	1
	Pass-through voltage, option B, TBD	Ion clearing voltage	2
Pulse flatness	peak-to-peak ripple	< 100 V	1
Stability at zero volts	HV output pulse flat top	< 100 V	1
Output Load			
Kicker plate capacitance	Including cables	< 100 pF	1
Input / Output Chassis Signals			
Trigger (input)	Controls TCLK trigger input, Mode 2 only. Rising edge triggers beam output, rear panel.	TTL, 50 Ohm internally terminated	1
nReady (output)	Controls read back, indication that all fault status bits are cleared and the Driver is capable and ready, rear panel.	Closed contact	2
HV_DC_OK (output)	Output to machine protection system, Indication that -5 kV	TTL, driven by 50	2

	DC PS is greater than -5 kV, rear panel.	Ohm driver	
Permit (input)	Input from machine protection sys., logic level high enables & low disables beam, rear panel.	TTL, 50 Ohm internally terminated	1
HV Output	Local monitor, analog, BNC front panel	1000:1	1
Beam Sync (output)	Monitor, digital, BNC rear panel	TTL, driven by 50 Ohm driver	2
MPS In	Mode setting command received from the MPS	TTL, 50 Ohm term.	3
MPS Out	Acknowledgement signal sent back to the MPS	TTL, 50 Ohm drive	3
Remote Control Over Ethernet (ACNET)			
Mode (read back only)	Operating Modes 0 through 4. 0 – not ready, 1 – ready and no beam, 2 – TCLK controls triggering, 3 – free running, 4 – DC beam. Mode 0 is not settable.	Integer value is the Mode	1, 3
Pulse width control	Settable parameter.	1 μs to 65,000 μs	1, 2
Free running frequency	Free running triggers. Test purpose only	1 to 60 Hz	2
Control bits	Reset, manual trigger	Digital	2
Status	Ready (summation), Behlke fault, HC DC PS OK, permit	Digital	2
Output voltage monitor	Analog read back, full scale range	0 to -6.5 kV	2
-5 kV PS monitor	Analog read back, full scale range	0 to -6.5 kV	2

Notes:

The following indicate the origination of the specification.

1. L. Prost, S. Shemyakin, Considerations for the Design of the LEBT Chopper for PXIE, Rev. A, Project X Doc 1219-v1 , Project X DocDB: http://projectx-docdb.fnal.gov

2. Added feature for system functional completeness and or ease of use.

3. 1/20/2016 Controller code changed to allow mode to be set only by the MPS and not directly by user.

1.2 Chopper Driver Operational Features

This section describes the basic Driver operating features. Interface control, at least initially, will be by way of a LabView application described in section 2.1.

All references to a "trip" are events resulting in the Driver advancing to Mode 0. The event causing the trip will indicate in the list of latched Status bits, assuming the condition is one of those items identified in and documented here.

1.2.1 Driver "Ready" state

Certain conditions must be met for the Driver to allow beam. If the Driver is in a condition to allow beam, it is said to be "Ready". The Ready condition depends on the summation of the following hardware conditions:

A. The Behlke high voltage switch is not faulted.
B. Pulse width does not exceed the pulse period.
C. The external Permit must be asserted.
D. The high voltage DC power supply must be at least -5.0 kVdc.

Note that each of these fault conditions is latched. Thus, the user will always be able to determine the reason for a trip, even if the fault was momentary. The user must clear fault indications by issuing a control bit "Reset" in order to operate in any of the operating modes.

The Ready state is a summation of several conditions. Ready and each conditions are read back as "status" and described below.

Chassis Ready — This condition is a summation of parameters A thru D above. The Ready condition is brought out on a chassis connector intended to be routed to Controls. See Table 1.2 for the electrical specifications of this chassis output signal.

Behlke OK — The internal commercial HV switch has a fault status bit and is included in the Ready state summation.

Pulse Width OK — This condition is detected only in Mode 2 operation. Pulse widths that are longer than the period of external TCLK triggers are detected and cause a trip of this status condition. Pulse width can be a problem, because the width is set independently from the external TCLK triggers rep rate; and the trigger period may be too short for the pulse width.

Permit — This is an input signal to the Driver chassis that must be continuously asserted to allow beam to be pulsed. This signal originates from a Controls subsystem. Within 150 ns of Permit being dropped, the Driver will cut off the beam. See Table 1.2 for the electrical specifications of this chassis input signal.

HV DC PS — The "normal" state of the Chopper is to drive the chopper plate to -5 kVdc causing beam to be diverted to the absorber plate. The chopper plate driven to "0.0 Vdc" allows beam to proceed downstream. A comparator monitors the -5 kV PS and is set to trip if it drops below the magnitude of 5.0 kV. (Note that the chopper plate is connected not to 0.0 Vdc but about -300 Vdc when allowing beam to pass for the purpose of clearing ions.)

1.2.2 Operating modes

The Chopper Driver has five operational modes. The Driver state of readiness, as described above, as well as the user's choice determine the operational mode. Four of the five modes are user selectable. The mode is an analog setting parameter.

Mode 0: This mode is entered automatically whenever the Driver's operating condition is not Ready. In mode 0, the kicker plate is clamped to -5 kV. Monitoring system status will indicate the cause for not being Ready. Issuing a Reset will clear all fault indications - if the fault itself has cleared. Should the fault be cleared and the user issues a reset, then the mode will advance to 1. Note that the mode will not automatically advance to Mode 1 if a fault condition goes away on its own.

Mode 1: The Driver enters Mode 1 when all faults are cleared and the user has issued a Reset. In this mode the chassis Ready output signal will indicate and the Driver output remains clamped to -5 kV. The user must set the operating mode to either 2, 3 or 4 to allow beam to pass through the chopper. Selecting Mode 1 when in 2, 3 or 4 shuts beam off by deflecting it to the absorber.

Mode 2: The Driver responds to external TCLK triggers in this mode. Allowable external trigger rates are any rate up to and including 60 Hz. The "Pulse Width OK" condition is monitored in this mode.

Also, it is in this mode that the user can issue one-shot triggers by way of actuating control bit 1. Refer to Table 3.5.

Mode 3: This is the free-running pulse mode. The pulse rate is set as an analog setting parameter in the range of 1 to 60 Hz, inclusive. Bench testing the Driver is its intended purpose.

Mode 4: DC beam operating mode. The Chopper's plate voltage remains at a voltage near ground indefinitely.

The user is free to change operating modes between 1 through 4 -- at will -- as long as the Driver is in the Ready state.

1.2.3 Misc. Operating features

1. The pulse width and pulsing rep rate can be changed at any time.

2. The controller will not accept a value of rep rate from the user whose period is shorter than the current value of pulse width.

3. The controller will not accept a value of pulse width to be longer than the period of the repetition rate currently set. There exists a potential problem in Mode 2, because the repetition rate is determined by the TCLK trigger in the control system but the pulse width is set in the Chopper Driver. The period of TCLK triggers could be set to be too short for the currently set pulse width. Therefore, the controller is designed to trip when a TCLK trigger occurs while the HV output is still on. The status bit "Pulse Width Is OK" will show this trip.

1.3 Chassis I/O Connections

Table 1.2 lists the chassis input and output connections other than 120 VAC power connector.

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Table 1.2. Chassis connectors.

Signal	Input or output	Description
Rear Panel		
HV Out	Output	Reynolds 20kV, Chopper Driver output to deflector plate
-5 kV DC In	Input	SHV, HV DC deflection voltage input from external PS
-300 V DC In	Input	SHV, ion clearing voltage input, option B operation
Permit	Input	BNC, 50 Ohm terminated, TTL. A logic high permits beam and is required for operation in modes greater than Mode 0.
Trigger	Input	BNC, 50 Ohm terminated, TTL. A rising edge triggers a pulse of beam.
Beam Sync	Output	BNC, 50 Ohm, TTL. High level coincident with beam pulse. The actual HV switch closes 150 ns after the rising edge of Beam Sync.
nReady P:L21MOQ	Output	Contact closer indicates a "Ready" condition on a BNC connector. It is a summation of conditions. See Section 1.2.1. The contact current limit is about 10 mA having a voltage drop of 1.2 V.
HV_DC_OK P:L21MOQ	Output	BNC, 50 Ohm, TTL. A high level indicates the deflection voltage is greater than -5.0 kV and satisfactory to cut beam off.
MPS In	Input	BNC, 50 Ohm terminated, TTL. Serial TTL protocol. Mode control command from the MPS. See Section 2.2.
MPS Out	Output	BNC, 50 Ohm, TTL. Serial TTL protocol. Acknowledgement signal back to the MPS. See Section 2.2.
Front Panel		
Ethernet	In & out	RJ-45 connector.
Output Monitor	Output	BNC, deflector plate voltage monitor, 1kV/V, DC coupled
LOTO Test Point	Output	-5kV/V deflection HV DC PS monitor
LOTO Test Point	Output	-100V/V ion clearing VDC monitor, option B operation only

1.4 Front Panel LED Indications

Table 1.3. Front panel LED indications.

LED	LED No.	LED On Designation
Permit	LED8	Permit is enabled
Beam	LED7	Beam is not chopped out. Blinks on pulsed beam, continuously on for DC beam
Mode 3	LED6	Free running pulse mode
Mode 2	LED5	Externally triggered by TCLK
Ethernet communication received	LED4	Blinks when incoming Ethernet command received
Ethernet error in reception(1)	LED3	Blinks when some error with Ethernet or MPS command
Driver Ready	LED2	Driver status is ready for pulsed or DC beam
Heart beat, 1/2 Hz	LED1	Internal CPLD logic is functional

Notes:

(1) The red Ethernet Error LED indicates on two conditions: Ethernet error as well as an indication of an error regarding reception of the mode command coming from the MPS card. If the MPS sends a mode number that is an invalid value this LED will blink. Also, if there is no signal at all coming from the MPS, this LED will blink at a 10 Hz rate.

2 CHOPPER DRIVER CONTROL

2.1 Using The LabView Application RabbitUI For Control

Control of the Chopper Driver is by way of the RabbitUI LabView application. This program interfaces to a number of specific accelerator devices. Therefore, the first thing the user needs to do upon starting this application is choose the Chopper Driver to control. To do this click on the drop-down box under "Rabbit System Hostname" and select "LEBTChopper.fnal.gov" from the list.

This LabView application's interface design is taken from ACNET philosophy. The Chopper Driver has readings, settings, status and control data associated with its control. Data is arranged into four arrays for the purpose of communication between a network "client", in this case the LabView application or an ACNET parameter page, and the Chopper Driver chassis acting as a network "server". Settings can be both sent to the Driver and read back, so this brings the count to five possible "actions" corresponding to the five tabs on the application's interface. Some explanation of the control functions on these five tabs is in order.

Read — There are two readings, namely, the voltage of the high voltage power supply in the Driver and the output voltage. (These two voltages had better be the same when beam is cut off or something is wrong.) The voltage is fixed is read back. There are two readings and are listed in Table 3.2.

Read setting — Settings values are read back. Selections must be made in the two pull-down menus to observe the list of settings. The two pull-down menus are labeled "Initial Element" and "Final Element". Select the top element in the Initial list and the last element in the "Final" list. Then depress the "Read setting" button to view the values. The readable settings are the same as the list of settable parameters listed in Table 3.3.

Read status — Status bits are read back. There are labels identifying each status bit. Furthermore, status is arranged in groups of 16 digital words in the case of systems having a lot of status. Similar to the pull-down boxes in "Read setting", pull-down boxes provide

the means to select status displayed from all available status bits. For this Chopper Driver, there is only one status word, so there is only one word to choose from with the drop down selections. The status bits are listed in Table 3.4.

Set a setting — Settable parameters are controlled one at a time. Thus, select the desired parameter from the "Element" list. This tab provides the ability to enter either a scaled or raw (unscaled 16-bit integer) value. Enter a value in one of the two text boxes, then click the corresponding blue button. The blue box "Read Current Values" provides the means to read back what is now in the chosen element. Again, settings are listed in Table 3.3.

Set a control bit — Control bits are also arranged in an array of 16-bit words. The "Element" list is used to select the desired word of bits. (Typically there aren't many control bits in an application.) Only one control bit should be set at a time. Select only one bit to be on and click "Set a control bit". The list of control bits is in Table 3.5.

2.2 MPS Control of the Operating Mode

Control of the Chopper Driver is by way of communication over Ethernet, as described in Section 3.0, with one exception. In January 2016 a change was made to the Chopper to provide the best assurance of machine protection. The MPS hardware was made to communicate with the Chopper for it to exclusively allow changes to operating modes that allow beam to pass. The MPS sends commands to the Chopper Driver chassis using TTL serial protocol when it accepts the user's request to change the operating mode. Read back of the current mode number setting remains via the ACNET host node – and not the MPS.

The MPS mode value command code is a single byte. The Chopper returns the received code back to the MPS with each reception, whether a valid or otherwise. Both signals are sent with two stop bits and at 9600 baud. The MPS sends the user selected, and accepted, mode to the Chopper at a continuous rate (something like 2 or 5 Hz). The functionality of the controller operation and response to status trips remains the same as described in Section 1.2.2. The codes issued by the MPS are:

Table 2.1. MPS mode command code.

Code (one byte)	Mode No.
0x41	1
0x42	2
0x44	3
0x48	4

3 ETHERNET COMMUNICATION

The Chopper Driver is controlled is by way of a LabView application over Ethernet. The network parameters for communicating with the Driver chassis are given in Table 3.1.

Table 3.1. Driver chassis network parameters.

Network parameter	Value
Domain Name	LEBTChopper.fnal.gov
IP Address	131.225.142.166
Local Port	4524
Network Mask	255.255.255.0
Gateway	131.225.142.200

3.1 Ethernet Client/Server Communication Data Structures

The convention for communication between the Driver chassis and the LabView application is by implementing the protocol spelled out in the document *The Compact Ethernet Communication (CEC) Protocol*, Beams-doc_2109-v1. In conformance with this protocol, four data arrays are defined for the Driver and are shown in Tables 2.2 through 2.5.

The Rabbit RCM responds to requests over Ethernet and is therefore a server. The network device making requests will be referred to in the rest of this document as the "client".

The ADC full scale analog range is given in the Analog Range column from which to determine ACNET analog scale factors. The analog binary codes are 16-bit unsigned, unipolar for the ADC and DAC values.

There is one reading (Table 3.2 element number 2) and one control bit (Table 3.5 element 0, bit 3) that are only for diagnostic purposes that will may not necessarily be incorporated into ACNET parameters. These were added Dec. 30, 2014 to determine the reason for rare nuisance HV PS trips. These will be at least accessible via the LabView application.

Table 3.2. Array of analog readings. Used for Message Type Code 0.

Element No.	ACNET Parameter	Device Description	Displayed Units	Analog Range 0x0000 - 0xFFFF
0	P:L20MOV	High voltage PS	Vdc	-6500 to 0
1	P:L20MOU	Driver output voltage	Vdc	-6500 to 0
2	NA	Total HV PS trip counts	none	0 to 65535

Table 3.3. Array of analog settings. Used for Message Type Codes 1 & 3.

Element No.	ACNET Parameter	Device Description	Displayed Units	Analog Range 0x0000 - 0xFFFF
0	P:L20MOQ	Operating mode number. Valid modes are: 0, 1, 2 or 3.	none	Mode is integer value
1	P:L20MOH	Beam pulse width (Value 0 is not accepted.)	μs	0 – 16,665 as an integer value in the range
2	P:L20MOF	Free running pulse frequency. Mode 2 operation only. (Value 0 is not accepted.)	Hz	1 - 60 as an integer value in the range

Table 3.4. Array of status. Used for Message Type Code 2.

Element Number	Data Bit	Device	ACNET Parameter
0	0	Modulator Ready (1 = True, 0 = False)	P:L20MOQ
	1	Behlke switch is not faulted (1 = OK, 0 = Fault)	P:L20MOQ
	2	Pulse width is OK, i.e. pulse width is less than pulse period (1 = OK, 0 = Error)	P:L20MOQ
	3	Chopper chassis: Permit (1 = Enable, 0 = Disable)	P:L20MOQ
	4	Chopper: HV DC PS is on (1 = On, 0 = voltage too low)	P:L20MOQ

Table 3.5. Array of control. Used for Message Type Code 4. A bit set to 1 performs the function. The user must set only one of the following bits per issued command.

Element Number	Data Bit	Device	ACNET Parameter
0	0	Reset (1 = reset). Used to clear all trip/fault latches.	TBD
	1	Manual Trigger, in mode 2 only (1 = trigger)	TBD
	2	Interrupt 1 acknowledge sent from Rabbit RCM to PLD when pulse fired (1 = ack). Internal use only.	NA
	3	Reset total HV PS trip counts	NA

4 CIRCUIT DESCRIPTION

The controller in the Driver chassis is a three-PCB assembly located in the low voltage section of the chassis. The first board of the three-board controller is a configurable digital board referred to as a Modular Ethernet Communication (MEC) board. Its two major components are a commercial 8-bit computer on a sub-credit card size PCB and a complex programmable logic (CPLD) IC. The computer board is a Rabbit Core Module (RCM) model RCM3010 with Ethernet capability. The CPLD is an Altera MAX II family EPM1270. The second board of the assembly is a data acquisition board with 16 channels of 16-bit ADC and 4 channels of 14-bit DAC. The third board interfaces with the HV DC PS in the chassis.

4.1 Device Addressing

This section documents a convention employed for communication between the computer RCM and the CPLD on the digital controller board. The RCM has a total of 56 general purpose I/O lines (GPIO), most of which are configurable.

The Driver's circuitry is composed of "devices" that need to be controlled. Devices can be either firmware coded into the CPLD or hardware ICs. The RCM reads and writes to defined registers in the CPLD to control devices. ICs such as a multi-channel A/D and D/A converters are each a device. Also, things such as pulse width control and status registers are also defined devices. Each device is assigned a register address, and the RCM reads from and writes to these registers.

The concept of an address and data bus is quite conventional, but it is worth mentioning that using a bus for control with external hardware is an optional RCM feature. Specific C language commands are issued to set up specific GPIO lines to implement this bus feature. The RCM subsequently writes to and reads from defined registers in the CPLD via this bus, but other GPIO lines are used for control as well. Rabbit documentation refers to the use of its external bus as the "external I/O" and also "auxiliary I/O" bus, depending where you are reading in the documentation. This external I/O bus is composed of an 8-bit data bus, a 6-bit address and two strobe lines—a read and a write. These GPIO lines are shown on the Appendix Fig. 1 diagram interconnecting the RCM with the CPLD.

4.2 Register Definitions and RCM to CPLD Interface signals

Table 4.1 shows the registers defined in the CPLD that the RCM reads from and write to. Note that although the RCM external/auxiliary I/O bus only contains 6 bits of address, Table 4.1 Address column shows16 bits. Per the Rabbit RCM design, writing to the higher address bits sets the strobe type to be used. Strobes need to be configured, and those configured are listed in Table 4.3. The Table 4.1 Address column correlates with Table 4.2 Address Range. Writing to a specific address range defines which strobe will be issued.

Table 4.1. Device registers defined in the CPLD . The Read/Write indication is with respect to RCM control. All registers are 8 bits. Strobe PE4 is used on all writes, PE5 is used on all reads.

Device Register	Comments		R/W	Address
Operating mode register	Setting, Table 3.3, values = 0, 1 or 2		W	0x8001
			R	0xA001
Pulse width, Unit of time is microseconds, Value is a 2-byte word	Setting, Table 3.3, LS byte		W	0x8002
	Setting, Table 3.3, MS byte		W	0x8003
Free-running pulse period, Unit of time is microseconds, Value is a 4-byte long word, Used in operating mode 2 only	Setting, Table 3.3, LS word	LS byte	W	0x8004
		MS byte	W	0x8005
	Setting, Table 3.3, MS word	LS byte	W	0x8006
		MS byte	W	0x8007
Status register	Table 3.4		R	0xA008
Control register	Table 3.5		W	0x8009
Total HV PS trip counts	Reading, Table 3.2, LS byte		R	0xA00A
	Reading, Table 3.2, MS byte		R	0xA00B

Also, several individual GPIO lines are used listed in Table 4.3. Refer to Appendix Tables A.2 and A.3 as a reference for the RCM port and pin alternate functions. The spread sheet column C, "Altera Pin", identifies which of the Alter EPM1270 CPLD pins have been interconnected to the RCM's I/O pins in the PCB layout. This spread sheet reveals what is available for configuration of any application, not the chopper has been configured.

Table 4.2. Strobe configurations. Address range relates to addresses shown in Table 3.1.

Bit	Type	Sense	Wait States	Address Range
PE4	Write	Active HI	1	0x8000 – 0x9FFF
PE5	Read	Active HI	1	0xA000 – 0xBFFF

Table 4.3. RCM general, configurable I/O lines used to interface with the CPLD. Direction of I/O is with respect to the RCM.

Bit	RCM Pin	CPLD Pin	Function	RCM In/Out	
PB0	J2/2	5	SPI clock. Configured for alt. function CLKB	Out	
PC5	J1/20	6	SPI MISO, master in slave out. PC5 is configured for alt. function RxB	In	
PC4	J1/19	7	SPI MOSI, master out slave in. PC5 is configured for alt. function TxB	Out	
PE6	J2/14	3	ADC chip select line	Out	
PE7	J2/13	4	Client-issued chassis reset, issued to the CPLD as a one-shot	Out	
PF5	J2/10	140	Enable/disable beam (1 = Enable, 0 = Disable), latched in the CPLD. Read back as status bit 1.	Out	
PF4	J2/9	141	User-issued manual trigger, mode 2 only, issued to the CPLD as a one-shot	Out	
PE4	J2/16	1	STR4, Strobe 4, RCM write	Out	
PE5	J2/15	2	STR5, Strobe 5, RCM read	Out	
PE1	J2/18	143	Interrupt 1 line, active high (1)	In	

(1) See chapter 7 in the Rabbit 3000 Microprocessor User's Manual, 019-0108_Z, per external interrupts.

4.3 Analog Voltages Read Back

The data acquisition board, the modified ED-385130, performs D/A conversion for the read back of the signals listed in Table 3.2 -- internal HV DC power supply and the HV output voltage. The output voltage should be the voltage of the HV DC PS when the chopper is cutting off the beam, and it will be zero volts when the beam is allowed to pass through the chopper.

The D/A conversion of HV output voltage is sampled within microseconds of the chopper trigger, so it will correctly show the output voltage of zero volts only if the pulse width is greater than about 10 μs wide. The reason is that it takes this long to perform the voltage conversion. Otherwise for narrower pulses, the voltage read back will not be zero but some negative value. This board's channel 3 measures the output voltage, and channel 4 measures the HV DC PS (where the channels are numbered 1 – 16).

These signals are scaled to provide maximum resolution and minimize noise. The D/A converter used has an input analog voltage range of 0 to 4.096 V. The gain and offset voltage for these analog signals have been set so that an input voltage of -6.50 V to 0 maps to the ADC input voltage of 0 to 4.096 V, respectively. The offset voltage used, namely +4.096 Vdc, had to be provided by way of a kludge wire to both of these channels.

APPENDIX SECTION A.

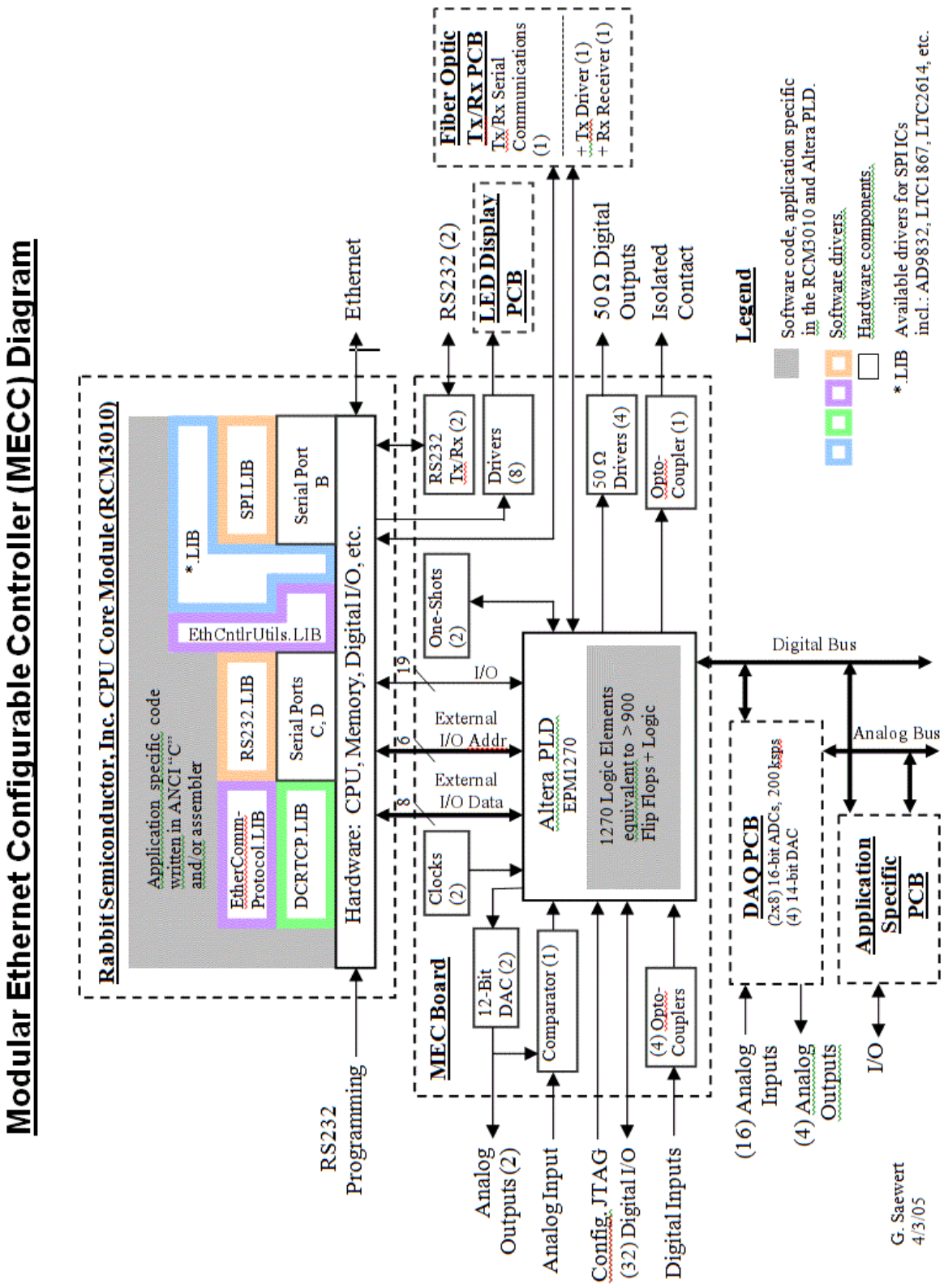


Fig. A.1. Controller assembly block diagram. Refer to the text for a description of those features used in the Chopper Driver Controller.

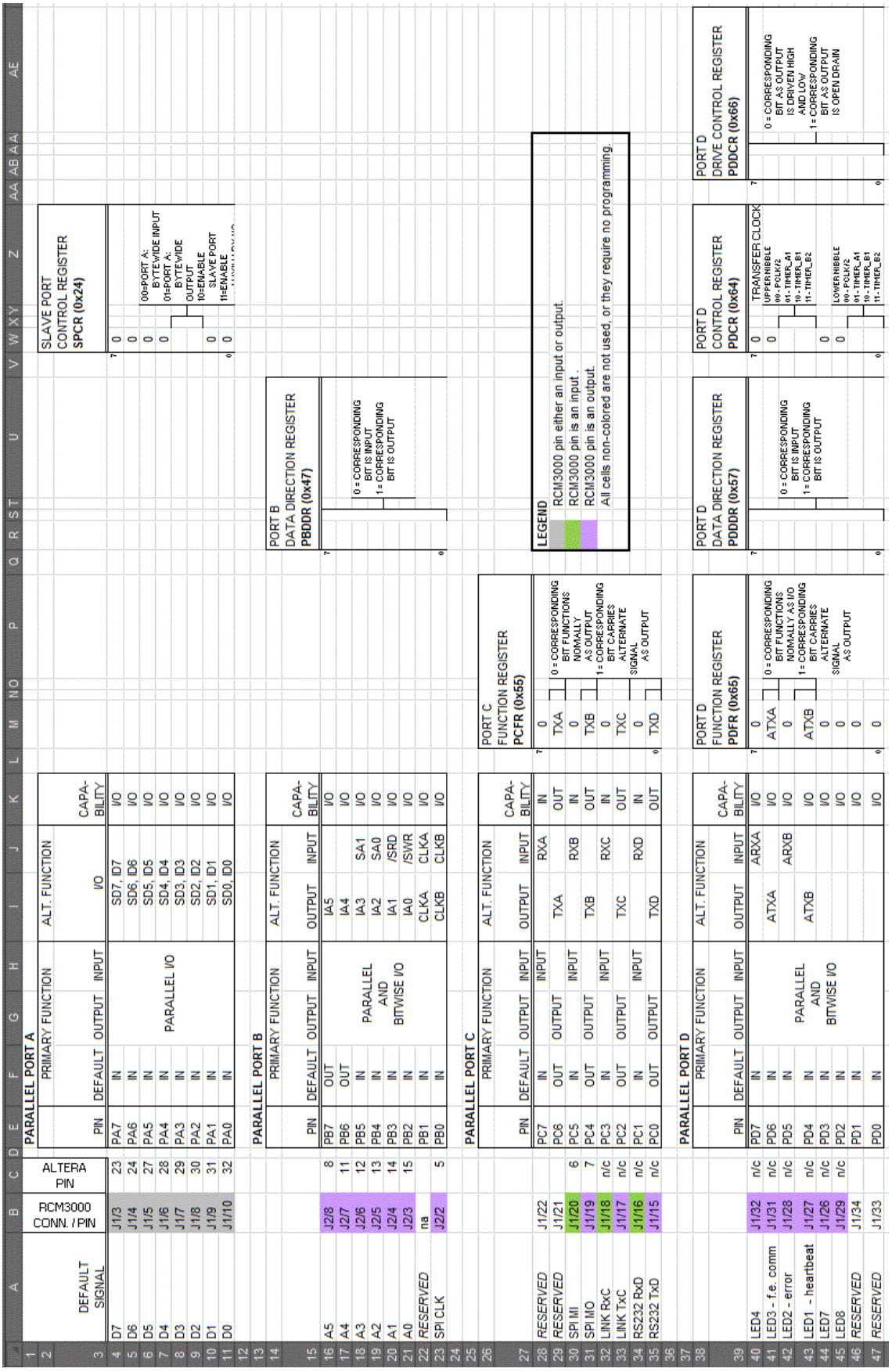
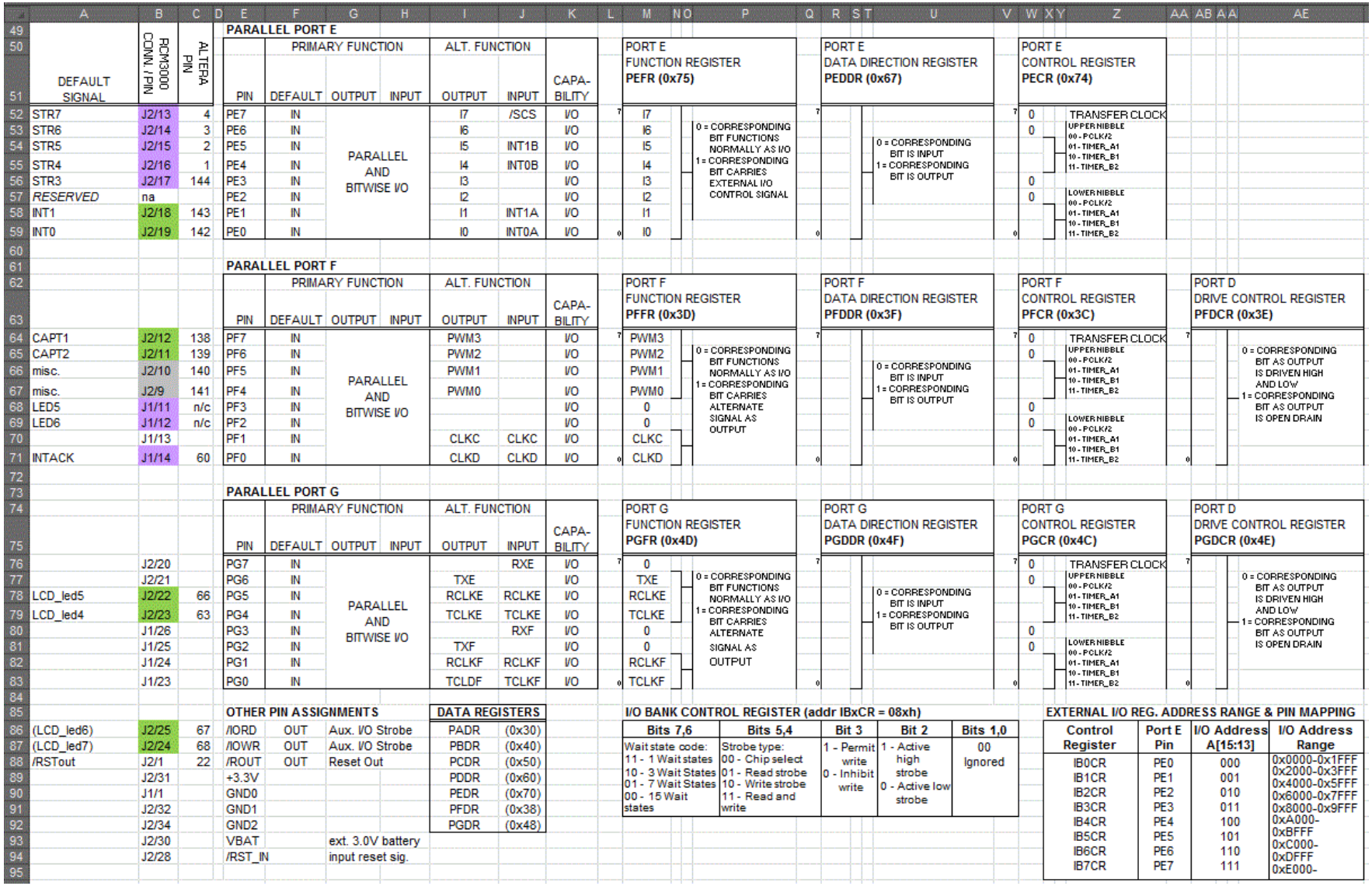


Fig. A.2. RCM port and pin definitions. Full functionality is shown. Refer to the text for those pins used. Columns B and C are the wiring connections between the RCM module and the CPLD.



PARALLEL PORT E

DEFAULT SIGNAL	RCM3000 CONN / PIN	ALTERA PIN	PRIMARY FUNCTION PIN	PRIMARY FUNCTION DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPABILITY
STR7	J2/13	4	PE7	IN	PARALLEL AND BITWISE I/O		I7	/SCS	I/O
STR6	J2/14	3	PE6	IN			I6		I/O
STR5	J2/15	2	PE5	IN			I5	INT1B	I/O
STR4	J2/16	1	PE4	IN			I4	INT0B	I/O
STR3	J2/17	144	PE3	IN			I3		I/O
RESERVED	na		PE2	IN			I2		I/O
INT1	J2/18	143	PE1	IN			I1	INT1A	I/O
INT0	J2/19	142	PE0	IN			I0	INT0A	I/O

PORT E FUNCTION REGISTER **PEFR (0x75)**: 7 I7 … 0 I0 — 0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O; 1 = CORRESPONDING BIT CARRIES EXTERNAL I/O CONTROL SIGNAL

PORT E DATA DIRECTION REGISTER **PEDDR (0x67)**: 0 = CORRESPONDING BIT IS INPUT; 1 = CORRESPONDING BIT IS OUTPUT

PORT E CONTROL REGISTER **PECR (0x74)**: 7 TRANSFER CLOCK; 6 UPPER NIBBLE; 5 0; 4 LOWER NIBBLE; 3 0; 2–0 — 00 - PCLK/2, 01 - TIMER_A1, 10 - TIMER_B1, 11 - TIMER_B2

PARALLEL PORT F

PIN	DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPABILITY
PF7	IN	PARALLEL AND BITWISE I/O		PWM3		I/O
PF6	IN			PWM2		I/O
PF5	IN			PWM1		I/O
PF4	IN			PWM0		I/O
PF3	IN					I/O
PF2	IN					I/O
PF1	IN			CLKC	CLKC	I/O
PF0	IN			CLKD	CLKD	I/O

PORT F FUNCTION REGISTER **PFFR (0x3D)**: 7 PWM3 … 0 CLKD — 0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O; 1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

PORT F DATA DIRECTION REGISTER **PFDDR (0x3F)**: 0 = CORRESPONDING BIT IS INPUT; 1 = CORRESPONDING BIT IS OUTPUT

PORT F CONTROL REGISTER **PFCR (0x3C)**: 7 TRANSFER CLOCK; 6 UPPER NIBBLE; 5 0; 4 LOWER NIBBLE; 3 0; 2–0 — 00 - PCLK/2, 01 - TIMER_A1, 10 - TIMER_B1, 11 - TIMER_B2

PORT D DRIVE CONTROL REGISTER **PFDCR (0x3E)**: 7 — 0 = CORRESPONDING BIT AS OUTPUT IS DRIVEN HIGH AND LOW; 1 = CORRESPONDING BIT AS OUTPUT IS OPEN DRAIN

PARALLEL PORT G

PIN	DEFAULT	PRIMARY FUNCTION OUTPUT	PRIMARY FUNCTION INPUT	ALT. FUNCTION OUTPUT	ALT. FUNCTION INPUT	CAPABILITY
PG7	IN	PARALLEL AND BITWISE I/O			RXE	I/O
PG6	IN			TXE		I/O
PG5	IN			RCLKE	RCLKE	I/O
PG4	IN			TCLKE	TCLKE	I/O
PG3	IN				RXF	I/O
PG2	IN			TXF		I/O
PG1	IN			RCLKF	RCLKF	I/O
PG0	IN			TCLDF	TCLKF	I/O

PORT G FUNCTION REGISTER **PGFR (0x4D)**: 7 0 … 0 TCLKF — 0 = CORRESPONDING BIT FUNCTIONS NORMALLY AS I/O; 1 = CORRESPONDING BIT CARRIES ALTERNATE SIGNAL AS OUTPUT

PORT G DATA DIRECTION REGISTER **PGDDR (0x4F)**: 0 = CORRESPONDING BIT IS INPUT; 1 = CORRESPONDING BIT IS OUTPUT

PORT G CONTROL REGISTER **PGCR (0x4C)**: 7 TRANSFER CLOCK; 6 UPPER NIBBLE; 5 0; 4 LOWER NIBBLE; 3 0; 2–0 — 00 - PCLK/2, 01 - TIMER_A1, 10 - TIMER_B1, 11 - TIMER_B2

PORT D DRIVE CONTROL REGISTER **PGDCR (0x4E)**: 7 — 0 = CORRESPONDING BIT AS OUTPUT IS DRIVEN HIGH AND LOW; 1 = CORRESPONDING BIT AS OUTPUT IS OPEN DRAIN

OTHER PIN ASSIGNMENTS

(LCD_led6)	J2/25	67	/IORD	OUT	Aux. I/O Strobe
(LCD_led7)	J2/24	68	/IOWR	OUT	Aux. I/O Strobe
/RSTout	J2/1	22	/ROUT	OUT	Reset Out
	J2/31		+3.3V		
	J1/1		GND0		
	J2/32		GND1		
	J2/34		GND2		
	J2/30		VBAT		ext. 3.0V battery
	J2/28		/RST_IN		input reset sig.

DATA REGISTERS

PADR	(0x30)
PBDR	(0x40)
PCDR	(0x50)
PDDR	(0x60)
PEDR	(0x70)
PFDR	(0x38)
PGDR	(0x48)

I/O BANK CONTROL REGISTER (addr IBxCR = 08xh)

Bits 7,6	Bits 5,4	Bit 3	Bit 2	Bits 1,0
Wait state code: 11 - 1 Wait states 10 - 3 Wait States 01 - 7 Wait States 00 - 15 Wait states	Strobe type: 00 - Chip select 01 - Read strobe 10 - Write strobe 11 - Read and write	1 - Permit write 0 - Inhibit write	1 - Active high strobe 0 - Active low strobe	00 Ignored

EXTERNAL I/O REG. ADDRESS RANGE & PIN MAPPING

Control Register	Port E Pin	I/O Address A[15:13]	I/O Address Range
IB0CR	PE0	000	0x0000-0x1FFF
IB1CR	PE1	001	0x2000-0x3FFF
IB2CR	PE2	010	0x4000-0x5FFF
IB3CR	PE3	011	0x6000-0x7FFF
IB4CR	PE4	100	0x8000-0x9FFF
IB5CR	PE5	101	0xA000-0xBFFF
IB6CR	PE6	110	0xC000-0xDFFF
IB7CR	PE7	111	0xE000-0xE000-

Fig. A.3. RCM port and pin definitions continued.

APPENDIX SECTION B

This section includes some Rabbit Semiconductor documentation for convenience.

BitWrPortI <SYSIO.LIB>

SYNTAX: void BitWrPortI(int io_port, char *PORTShadow, int value, int bitcode);
KEYWORDS: parallel port
PARAMETER1: address of internal I/O port.
PARAMETER2: address of variable shadowing current value of port.
PARAMETER3: value to write to port.
PARAMETER4: bit (0-7) to write value to.
DESCRIPTION: Updates shadow register at bit with value (0 or 1) and copies shadow to I/O port. WARNING: a shadow register is REQUIRED for this function. All of the Rabbit internal registers have predefined macros corresponding to the register's name. PADR is #defined to be 0x30, etc.
RETURN VALUE: None

WrPortI <SYSIO.LIB>

SYNTAX: void WrPortI(int io_port, char *PORTShadow, int data_value);
KEYWORDS: parallel port
PARAMETER1: address of internal I/O port.
PARAMETER2: address of variable shadowing current value of port.
PARAMETER3: value to write to port.
DESCRIPTION: Writes an internal I/O port with 8 bits and updates shadow for that port. The variable names must be of form "Port" and "PORTShadow" for most efficient operation. A null pointer may be substited (use "NULL") if shadow support is not desired or needed. All of the Rabbit internal registers have predefined macros corresponding to the register's name. PADR is #defined to be 0x30, etc.

NOTE: This function is interruptible and shadow values should not be assumed to be safe if modified in user defined interrupts
RETURN VALUE: none

SetVectExtern3000 <SYS.LIB>

SYNTAX: unsigned SetVectExtern3000(int interruptNum, void *isr);
DESCRIPTION: Function to set one of the external interrupt jump table entries for the Rabbit 3000 CPU and some versions of the Rabbit 2000. All Rabbit interrupts use jump vectors. See SetVectIntern for more information.
PARAMETER1: External interrupt number. Two are possible -- 0 and 1 are the only valid values.
PARAMETER2: ISR handler address, ie pointer to a function. Must be a root address.
RETURN VALUE: 0 failed
!=0 NON-RABBITSYS: jump address in vector table
RABBITSYS: isr
SEE ALSO: GetVectExtern3000, SetVectIntern, GetVectIntern